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Claims

[c1] 1. A silicon storage apparatus, comprising:
a solid-state storage medium, adapted for storing a plurality of data; and
a controller, coupled to said solid-state storage medium;
wherein said controller receives a read signal topre-store a portion of the data therein which are other of said data required by the read signal.

[c2] 2. A controller of a silicon storage apparatus, comprising:
a processor;
a system interface, adapted for receiving an operation signal;
a memory interface, coupled to a solid-state storage medium;
a transmission buffer, coupled to said memory interface and said system interface; and
a cache buffer, overlapping said transmission buffer to couple to said memory interface and said system interface;
wherein when said operative signal is a read signal, said processor retrieves a address mapping table to store a

pre-storage data which is not indicated by said read signal intosaid cache buffer; and when said operative signal is a subsequent read signal, saidcache buffer stores a data, and said processor determines whether or not said data conform to said pre-storage data.

[c3] 3. The controller of a silicon storage apparatus as cited in claim 2, further comprising an allocation table buffer area, coupling to said system interface and said memory interface, adapted to store said address mapping table.

[c4] 4. The controller of a silicon storage apparatus as cited in claim 2, wherein said cache buffer and said transmission buffer alternately synchronously transmit data.

[c5] 5. A data transmission method of a controller of a silicon storage apparatus, said silicon storage apparatus comprising a transmission buffer, a cache buffer, an allocation table buffer area, a system interface and a memory interface, said method comprising:
receiving a first data required by a read signal by said transmission buffer;
storing a second data not indicated by the read signal intosaid cache buffer after the transmission buffer being saturated; and
comparing and determining whether said second data conform to a third data required requested by a subse-

quent read signal.

[c6] 6. The data transmission method of a controller of a silicon storage apparatus as cited in claim 5, wherein the step of determining whether said second data conform tosaid third data required by said subsequent read signal, further comprises:
outputting said second data from said cache buffer when said second data conform tosaid third data; and
removing said second data from said cache buffer when said second data does not conform to the third data.

[c7] 7. The data transmission method of a controller of a silicon storage apparatus as cited in claim 5, wherein the cache buffer comprises at least one minimum accessing unit, and said minimum accessing unit comprises at least one sector.

[c8] 8. The data transmission method of a controller of a silicon storage apparatus as cited in claim 5, wherein the cache buffer and the transmission buffer alternately synchronously transmit data.

[c9] 9. The data transmission method of a controller of a silicon storage apparatus as cited in claim 5, wherein when said system interface receives a write signal and a write data in response thereto, said processor writes said write

data into a solid-state medium according to a address mapping table; and when the process for writing data is completed, said address mapping table is written into said solid-state medium.

[c10] 10. The data transmission method of a controller of a silicon storage apparatus as cited in claim 9, wherein said cache buffer receives said write data transmitted from said system interface while said processor is decoding said write data signal; and when the process of said decoding is completed, said write data is written into said solid-state medium from said cache buffer through said memory interface.

[c11] 11. The data transmission method of a controller of a silicon storage apparatus as cited in claim 9, wherein the content of said address mapping table is renewed according to the transmission of said write signal; said processor writes said write data into said solid-state storage medium from said cache buffer through said memory interface; and when the process of said writing is completed, said address mapping table is written into said solid-state medium.